



07/357797

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR

UNITED STATES LETTER PATENT

FOR

SERIES-RESONANT INVERTER BALLAST

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, OLE KRISTIAN NILSEN, a citizen of Norway, residing at Caesar Drive, Route 5, Barrington, Illinois, County of Cook, United States of America, have invented a

61
SERIES-RESONANT INVERTER BALLAST

of which the following is a specification.



721-00 201 A
933891
07/35/79

BACKGROUND OF THE INVENTION

Related Applications

Instant application is a Continuation-in-Part of Serial No. 020,478 filed March 2, 1987; which is a Continuation-in-Part of Serial No. 262,542 filed May 5, 1981; which is a division of Serial No. 178,107 filed August 14, 1980, now abandoned.
Now U.S. Patent 4,857,546
Now U.S. Patent 4,845,943
U.S. Patent 4,602,516

P. R.
4/9/93
P. R.
5/1/93
S. C. L. L. C.
P

Field of Invention

Instant invention relates to inverter-type fluorescent lamp ballasting means operable to be powered from an ordinary electric utility power line.

SUMMARY OF THE INVENTION

CL

Objects of the Invention

CL

P

An object of the present invention is that of providing a reliable cost-effective fluorescent lamp ballasting means.

This as well as other objects, features and advantages of the present invention will become apparent from the following description and claims.

CLW

P

Brief Description

3

In its preferred embodiment, instant invention comprises a half-bridge inverter powered from an ordinary electric utility power line by way of a full wave rectifier-filter means. The high frequency squarewave voltage output of the inverter is loaded with a series-combination of a tank inductor and a tank capacitor, with a fluorescent lamp being connected in parallel with the tank capacitor. The ON-time (or forward conduction period) of each of the inverter's two transistors is shorter than half the period of the high frequency voltage; thereby manifestly preventing the two transistors from conducting simultaneously; thereby, in turn, protecting the inverter from self-destruction in case of lamp failure.

DRCLuk
P

Brief Description of the Drawings

Fig. 1 schematically illustrates a compact, screw-in, self-ballasted fluorescent lamp assembly constructed on basis of the preferred embodiment of the invention.

Fig. 2 is a schematic diagram of the preferred embodiment of the invention.

1/4 R.2
11/9/93

Fig. 3, (4-d) illustrates the waveforms of various voltages and currents associated with the ballasting circuit of Fig. 2.

2

DECL

DESCRIPTION OF THE PREFERRED EMBODIMENT

P Fig. 1 illustrates a screw-in gas discharge lamp unit 10 comprising a folded fluorescent lamp 11 secured to an integral base 12. The lamp comprises two cathodes 13, 14 which are supplied with the requisite high operating voltage from a frequency-converting power supply and ballasting circuit 16; which, because of its compact size, conveniently fits within base 12.

B Circuit 16 is connected by leads 17, 18 to a screw-type plug 19 adapted for screw-in insertion into a standard Edison-type incandescent lamp socket at which ordinary 120Volt/60Hz power line voltage is available.

B In Fig. 2, a power supply 23 is connected with the 120Volt/60Hz power line voltage and provides a center-tapped DC output voltage for supplying a high-efficiency half-bridge inverter circuit 24. The inverter circuit is operable to provide B14 a high-frequency (20-30 kHz) high-magnitude current-limited voltage to a load 26, which actually represents fluorescent lamp 11 of Fig. 1.

B Power supply 23 comprises bridge rectifier 27 which connects with 120Volt/60Hz power line terminals 28, 29 and provides full-wave rectified power line voltage to two series-connected filter capacitors 34, 36; which filter capacitors are: i) connected together at a center-tap 37, and ii) connected between a positive B+ bus 38 and a negative B- bus 39.

31 Inverter circuit 24 is a half-bridge inverter comprising transistors 42, 43 connected in series between the B+ bus and the B- bus. The collector of transistor 42 is connected to the B+ bus 38, the emitter of transistor 42 and the collector of transistor 43 are connected to a midpoint line 44 ("M"), and 31 the emitter of transistor 43 is connected to the B- bus 39.

Midpoint line 44 is connected to center-tap 37 through a primary winding 46 of a toroidal saturable core transformer 47, a primary winding 48 on an identical transformer 49, a tank inductor 51 (L) and a series-connected tank capacitor 52 (C). Inductor 51 and capacitor 52 are energized upon alternate transistor conduction in manner to be described later. Load 26 is connected in parallel with capacitor 52.

Drive current to the base terminals of transistors 42 and 43 is provided by secondary windings 53, 54 of transformers 49, 47, respectively. Winding 53 is also connected to midpoint line 44 through a bias capacitor 56, while winding 54 is connected

31

to the B- bus 39 through an identical bias capacitor 57. The base terminals of transistors 42 and 43 are also connected to lines 38 and 44 through bias resistors 58 and 59, respectively. Shunt diodes 66 and 67 are connected across the collector-emitter terminals of transistors 42 and 43, respectively. A capacitor 68 is connected across the collector-emitter terminals of transistor 43 to restrain the rate of voltage rise across those terminals.

A first optional biasing arrangement BA1 comprises a diode 69 connected with its cathode to the base of transistor 42 and with its anode to the cathode of a diode 71 by way of a resistor 70; the anode of diode 71 is connected with the emitter of transistor 42 by way of a resistor 72; the cathode of diode 71 is connected with the un-dotted side of secondary winding 53 of transformer 49. A second optional biasing arrangement BA2 comprises a diode 73 connected with its cathode to the base of transistor 43 and with its anode to the cathode of a diode 75 by way of a resistor 74; the anode of diode 75 is connected with the emitter of transistor 43 by way of a resistor 76; the cathode of diode 76 is connected with the un-dotted side of secondary winding 54 of transformer 47.

The operation of the circuit of Fig. 2 can best be understood with additional reference to Fig. 3, which illustrates significant portions of the waveforms of the voltage at midpoint M (Fig. 3A), the base-emitter voltage on transistor 42 (Fig. 3B), the current through transistor 42 (Fig. 3C), and the capacitor 52 voltage and the inductor 51 current (Fig. 3D).

I

Starting at a point where transistor 42 first starts to conduct, current flows from the B+ bus 38 through windings 46 and 48 and inductor 51 to charge capacitor 52 and returns to the B+ bus through capacitor 34 (refer to the time period designated I in Fig. 3). When the saturable transformer 49 saturates at the end of period I, drive current to the base of transistor 42 will terminate, causing voltage on the base of the transistor to drop to the negative voltage stored on bias capacitor 56 in a manner to be described, causing this transistor to become non-conductive. As shown in Fig. 3c, current-flow in transistor 43 terminates at the end of period I.

However, since the current flowing through inductor 51 cannot change instantaneously, this current will now continue to flow from the B- bus 39 through capacitor 68, eventually causing the voltage at midpoint line 44 to drop to the voltage

4

3/

level on the B- bus (period II in Fig. 3). Thus, capacitor 68 restrains the rate of voltage change across the collector and emitter terminals of transistor 42.

3/

The current through inductor 51 reaches its maximum value when the voltage at midpoint line 44 is zero. During period III, the current will continue to flow through inductor 51 but will be supplied from the B- bus through shunt diode 67. It will be appreciated that during the latter half of period II and all of period III, positive current is being drawn from a negative voltage; which, in reality, means that energy is being returned to the power supply through a path of relatively low impedance.

When the inductor current reaches zero at the start of period IV, the current through the primary winding 46 of the saturable inductor 47 will cause a current to flow out of its secondary winding 54 to cause transistor 43 to become conductive, thereby causing a reversal in the direction of current through inductor 51 and capacitor 52. When transformer 47 saturates at the end of period IV, the drive current to the base of transistor 43 terminates and the current through inductor 51 will be supplied through capacitor 68, causing the voltage at midpoint 44 to rise (Period V). When the voltage at the midpoint line M reaches the voltage on the B+ bus, the current will then flow through shunt diode 66 (period VI). The cycle is then repeated.

As seen in Fig. 3, saturable transformers 47, 49 provide transistor drive current only after the current through inductor 51 has diminished to zero. Further, the transistor drive current is terminated before the current through inductor 51 has reached its maximum amplitude. This coordination of base drive current and inductor current is achieved because of the series-connection between the inductor 51 and the primary windings 46, 48 of saturable transformers 47, 49, respectively.

The series-connected combination of inductor 51 and capacitor 52 is energized upon the alternate conduction of transistors 42 and 43. With a large value of capacitance of capacitor 52, very little voltage will be developed across its terminals. As the value of this capacitance is decreased, however, the voltage across this capacitor will increase. As the value of capacitor 52 is reduced to achieve resonance with inductor 51, the voltage on the capacitor will rise and become infinite in a loss-free circuit operating under ideal conditions.

It has been found desirable to regulate the transistor inversion frequency, determined mainly by the saturation time of saturable transformers 47, 49, to be equal to or higher than

5

the natural resonance frequency of the inductor and capacitor combination in order to provide a high voltage output to external load 26.

Due to so-called Q-multiplication, a high-magnitude voltage develops across capacitor 52 as the transistor inversion frequency approaches the natural resonance frequency of the series-combination of inductor 51 and capacitor 52.

When inverter circuit 24 is used in the self-ballasted fluorescent lamp of Fig. 1, it has been found that the inversion frequency may be about equal to the natural resonance frequency of the series L-C tank circuit consisting of inductor 51 and capacitor 52. However, if the capacitance value of capacitor 52 is reduced below the point of resonance, unacceptably high transistor currents will result and transistor burn-out will occur.

The sizing of capacitor 52 is determined by the particular application of inverter circuit 24; but, as long as the combined load presented to the output of inverter transistors 42, 43, has an effective inductance value sufficient to provide adequate energy storage for self-sustained transistor inverter action, the current-feedback provided by saturable transformers 47, 49 will effect alternate transistor conduction without the need for additional voltage-feedback.

Because the voltages across transistors 42, 43 are relatively low (due to the absolute voltage-clamping effect of capacitors 34, 36), the half-bridge inverter 24 is very reliable. The absence of switching transients minimizes the possibility of transistor burn-out.

Inverter circuit 24 comprises means for supplying reverse bias to the conducting transistor upon saturation of its associated saturable transformer. For this purpose, capacitors 56 and 57 are charged to negative voltages as a result of reset currents flowing into secondary windings 53, 54 from the bases of transistors 42, 43, respectively. This reverse current rapidly turns off a conducting transistor to increase its switching speed and to achieve high inverter switching efficiency.

When a transistor base-emitter junction is reversely biased, it exhibits the characteristics of a Zener diode, having a reverse breakdown voltage on the order of 8 to 14 Volt for transistors typically used in high-voltage inverters.

Since load ²⁶56 comprises a fluorescent lamp, the maximum magnitude of the voltage across capacitor 52 will be limited by the lamp's ignition and operating characteristics, thereby effectively preventing voltages across inductor 51 and capacitor 52 from ever reaching destructive levels.

The above-presented explanation of the operation of the Fig. 2 inverter circuit was based on the two biasing arrangements (BA1 and BA2) being non-connected.

3
L
3
With these biasing arrangements actually connected as indicated, the inverter's operation will become independent of the exact magnitudes of the transistors' base-emitter Zenering voltages. Instead, the magnitude of the negative bias voltage established on each of capacitors 56 and 57 can now be chosen by choice of resistance value of resistor 72 and/or resistor 76: the lower the resistance value, the lower the magnitude of the associated negative bias voltage; and, in turn, the longer the transistors' ON-time, the lower the inverter's self-oscillating frequency, and the higher the magnitudes of the inverter's output current and power.

By providing for means whereby the resistance values of resistors 72 and 76 can be manually adjusted (in tandem and/or individually), the power provided to the fluorescent lamp may be correspondingly adjusted: the lower the resistance values, the more power provided to the lamp.

Moreover, due to the negative feedback effect inherently provided by resistors 72 and 74, the inverter may be made to operate safely even with the fluorescent lamp being non-connected.

3
3
L
This negative feedback effect is due to the fact that, as the magnitude of the current flowing through the L-C circuit increases, the magnitudes of the drive currents provided to the transistors' bases increase, and the magnitudes of the currents drawn out of capacitors 56 and 57 increase correspondingly; which, in turn, increases the magnitudes of the negative bias voltages present on these capacitors to the point where the magnitudes of the currents flowing through resistors 72 and 76 equal those of the increased base currents. However, the increased negative bias voltages will inherently shorten the transistors' ON-times; which, in turn, will increase the inverter frequency, thereby reducing the inverter's output current; etc. In other words, the indicated biasing arrangements provide for an automatic self-limiting of the magnitude of the inverter's output current.

CL
p
Additional Explanations and Comments

a) With commonly available components, inverter circuit 24 can be made to operate efficiently at any frequency between

a few kHz to perhaps as high as 50 kHz. However, for various well-known reasons (i.e., eliminating audible noise, minimizing physical size, and maximizing efficiency), the frequency actually chosen for the lamp unit of Fig. 1 was in the range of 20 to 30 kHz.

b) The fluorescent lighting unit of Fig. 1 could be made in such manner as to permit fluorescent lamp 11 to be disconnectable from its base 12 and ballasting means 16. However, if powered with normal line voltage without its lamp load connected, frequency-converting power supply and ballasting circuit 16 is apt to self-destruct.

To avoid such self-destruction, arrangements can readily be made whereby the very act of removing the load automatically establishes a situation that prevents the possible destruction of the power supply and ballasting means. For instance, with the tank capacitor (52) being permanently connected with the lamp load (11) -- thereby automatically being removed whenever the lamp is removed -- the inverter circuit is protected from self-destruction.

c) At frequencies above a few kHz, the load represented by a fluorescent lamp -- once it is ignited -- is substantially resistive. Thus, with the voltage across lamp 11 being of a substantially sinusoidal waveform (as indicated in Fig. 3d), the current through the lamp will also be substantially sinusoidal in waveshape.

d) In the fluorescent lamp unit of Fig. 1, fluorescent lamp 11 is connected with power supply and ballasting circuit 16 in the exact same manner as is load 26 connected with the circuit of Fig. 2. That is, it is connected in parallel with the tank capacitor (52) of the L-C series-resonant circuit. As is conventional in instant-start fluorescent lamps -- such as lamp 11 of Fig. 1 -- the two terminals from each cathode are shorted together, thereby to constitute a situation where each cathode effectively is represented by only a single terminal. However, it is not necessary that the two terminals from each cathode be shorted together; in which case -- for instant-start operation -- connection from a lamp's power supply and ballasting means need only be made with one of the terminals of each cathode.

e) It is noted that the transistor's ON-time is shorter than half the period of the inverter's high frequency squarewave voltage output; which voltage output is illustrated by Fig. 3A.

3
L

The fact that each of the transistors' ON-times is shorter than half the period of the inverter's high frequency output voltage (or output current) is important: it inherently provides for a situation where the two transistors are manifestly prevented from conducting at the same time, thereby providing protection against circuit failure due to excess-magnitude transistor currents.

f

f) By adjusting the resistance values of resistors 72 and/or 76, the ON-times of the associated transistors are adjusted accordingly. For instance, by increasing the resistance value of resistor 76, the ON-time associated with transistor 43 is shortened; and, as a result, the magnitude of the current provided to the load 26 is reduced.

g

g) It is thought that the present invention and many of its attendant advantages will be understood from the foregoing description and that many changes may be made in the form and construction of its components parts, the form described being merely a preferred embodiment of the invention.

9